As a result, the data stored in the first latch circuit LAT(A) connected to the memory cell which is being written into to bring the data in the memory cell into state "7" is kept at write data "0" according to the data stored in the second latch circuit. Then, the data is changed to data "1" which allows only the first latch circuit LAT(A) connected to the memory cell whose data has been written to obtain state "6" to show verify OK.

In this way, the third-page write operation and verify operation are repeated until the data in all the first latch circuits LAT(A) have become "1".

Next, the read operation will be explained. The data in the memory cell is read from the third page, second page, and first page in that order. The data in the memory cell and the data to be written onto and read from the first, second, and third pages have been defined as shown in FIG. **24**. Therefore, in the third-page read operation, if the data in the memory cell is "3" or less, the data read out will be "1". If the data in the memory cell is "4" or more, the data read out will be "0". This enables the data to be read in one read operation.

In the second-page read operation, if the data in the memory cell is either "1" or less or "6" or more, the data read out will be "1". If the data in the memory cell is "2" or more and "5" or less, the data read out will be "0". This enables the data to be read in two read operations.

In the first-page read operation, if the data in the memory cell is "0" or less, or "3" or more and "4" or less, or "7" or more, the data read out will be "1". If the data in the memory cell is "1" or more and "2" or less, or "5" or more and "6" or less, the data read out will be "0". This enables the data to be read in four read operations.

With the second embodiment, in the third-page write operation, as a result of the first-page and second-page write operations, the memory cell whose data is in state "0" is brought into state "7", the memory cell whose data is in state "1" is brought into state "6", the memory cell whose data is in state "2" is brought into state "5", and the memory cell whose data is in state "3" is brought into state "4". Consequently, the number of read operations on the first page is one, the number of read operations on the second page is two, and the number of read operations on the third page is four. Therefore, the number of reads from the first page is reduced as in the first embodiment.

Furthermore, the write operation that brings a memory cell whose data is in state "0" into state "7", the write operation that brings a memory cell whose data is in state "1" into state "6", the write operation that brings a memory cell whose data is in state "2" into state "5", and the write operation that brings a memory cell whose data is in state "3" into state "4" can be carried out simultaneously. Moreover, in these write operations, a higher initial write voltage than that used in a conventional equivalent can be used, enabling a higher-speed write operation.

(Third Embodiment)

FIG. **26** schematically shows the operation of an n-valued nonvolatile semiconductor memory device according to a third embodiment of the present invention. In this case too, data is written, starting from the first page, as in the first and second embodiments. Then, when the n-th page is written into, if the write data is "0", a memory cell whose data is in state "0" is brought into, for example, maximum state "x". In addition, a memory cell whose data is in state "1" is brought into state "x−1". From this point on, the maximum state "i" of the data written in the (n−1)th page write operation is brought into state "i+1".

In the third embodiment, the threshold voltage of the cell has been raised by the program operation and lowered by the erase operation. The present invention is not limited to this. For instance, the present invention may be applied to a nonvolatile semiconductor memory device where the threshold voltage of the cell is lowered by the program operation and raised by the erase operation.

Furthermore, the first and second latch circuits LAT(A) and LAT(B) have been composed of clocked inverter circuits. The present invention is not restricted to this. For instance, the first and second latch circuits LAT(A) and LAT(B) may be composed of capacitors and transistors that control the charging and discharging of the capacitors.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a data storage circuit which is connected to said bit line and stores not only data of a first or a second logical level externally supplied but also the data of the first or second level read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit operates in such a manner that

in a first operation, the control circuit changes the data in said memory element from said state "0" to state "1" when the data in said data storage circuit is data of the first logical level and keeps the data in said memory element in said state "0" when the data in said data storage circuit is data of the second logical level,

that in a first verify operation of verifying whether said data has reached state "1", the control circuit brings the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and said data has reached state "1", keeps the data in said data storage circuit at the first logical level when said data has not reached state "1", keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and carries out said first operation until the data in said data storage circuit has reached the second logical level, and

that in a second operation, the control circuit changes the data in said memory element from state "1" to state "2" when the data in said data storage circuit is data of the first logical level externally supplied and the data in said memory element is in state "1", and changes the data in said memory element from state "0" to state "3", when the data in said memory element is in state "0".

2. The nonvolatile semiconductor memory device according to claim **1**, wherein

said control circuit, in a second verify operation of verifying whether the data in said memory element has

reached state "2", brings the data in said data storage circuit to the second logical level when the data has reached state "2" in a case where the data in said data storage circuit is at the first logical level and the data in said memory element is in state "1" before said second operation is carried out, keeps the data in said data storage circuit at the first logical level when the data has not reached state "2", prevents the logical level in said data storage circuit from changing when the data in said memory element is in state "0" before said second operation is carried out, and keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and furthermore

said control circuit, in a third verify operation of verifying whether the data in said memory element has reached state "3", brings the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and the data has reached state "3", keeps the data in said data storage circuit at the first logical level when the data has not reached state "3", keeps the data in said data storage circuit at the second memory logical level when the data in said data storage circuit is at the second logical level, and carries out said second operation, second and third verify operations until the data in said data storage circuit has reached the second logical level.

3. The nonvolatile semiconductor memory device according to claim **1**, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying whether said data has reached state "2" and omits the verify operation of verifying whether said data has reached state "2" in the latter half of the verify operation of verifying whether said data h as reached state "3".

4. The nonvolatile semiconductor memory device according to claim **1**, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "1".

5. The nonvolatile semiconductor memory device according to claim **1**, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", brings the potential on th e bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

6. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and store s one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a first storage circuit which is connected to said bit line and stores data of a first or a second logical level externally supplied;

a second storage circuit which is connected to said bit line and stores the data of the first or second level read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said first and second storage circuits, wherein

said control circuit operates i n such a manner that

in a first operation, the control circuit changes the data in said memory element from state "0" to state "1" when the data in said first data storage circuit is data of the first logical level and keeps the data in said memory element at said state "0" when the data in said first storage circuit is data of the second logical level,

that in a first verify operation of verifying whether said data has reached state "1", the control circuit brings the data in said first storage circuit to the second logical level when the data in said first storage circuit is at the first logical level and said data has reached state "1", keeps the data in said first storage circuit at the first logical level when said data has not reached state "1", keeps the data in said first storage circuit at the second logical level when the data in said first storage circuit is at the second logical level, and carries out said first operation until the data in said first storage circuit has reached the second logical level,

that in a second operation, the control circuit stores the data read from said memory element into said second storage circuit, changes the data in said memory element from state "1" to state "2" when the data in said first storage circuit is data of the first logical level externally supplied, changes the data in said memory element from state "0" to state "3" when the data in said memory element is in state "0", and keeps the data in said memory element when the data in said first storage circuit is data of the second logical level,

that in a second verify operation of verifying whether the data in said memory element has reached state "2", the control circuit brings the data in said first storage circuit to the second logical level when the data has reached state "2" in a case where the data in said first storage circuit is at the first logical level and the data in said memory element is in state "1" before the second operation is carried out, keeps the data in said first storage circuit at the first logical level when said data has not reached state "2", and brings the potential on the bit line to which the memory element is connected to the first logical level and the data in said first storage circuit to the first logical level when the data in said second storage circuit is at the second logical level in a case where the data in said memory element is in state "0" before said second operation is carried out, and

that in a third verify operation of verifying said data has reached state "3", the control circuit brings the data in said first storage circuit to the second logical level when the data in said first storage circuit is at the first logical level and said data has reached state "3", keeps the data in said first storage circuit at the first logical level when said data has not reached state "3", keeps the data in said first storage circuit at the second memory logical level when the data in said first storage circuit is at the second logical level, and carries out said second operation and second and third verify operations until the data in said first storage circuit has reached the second logical level.

7. The nonvolatile semiconductor memory device according to claim **6**, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying whether said data has reached state "2" and omits the verify operation of verifying whether said data has reached state "2" in the latter half of the verify operation of verifying whether said data has reached state "3".

8. The nonvolatile semiconductor memory device according to claim 6, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "1".

9. The nonvolatile semiconductor memory device according to claim 6, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", brings the potential on the bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

10. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of an n number of data items made up of state "0", state "1", . . . , state "n" ($3 \leqq n$ where n is a natural number);

a data storage circuit which stores data of a first or a second logical level externally inputted; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit, in a final write operation, charges state "0" of the smallest data stored in said memory element into state "n" of the largest data when the data in said first storage circuit is data of the first logical level externally supplied, and keeps the data in said memory element when the data in said first storage circuit is data of the second logical level.

11. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, in a second verify operation of verifying whether the data in said memory element has reached state "2", charges the data in said data storage circuit to the second logical level when the data has reached state "2", in a case where the data in said data storage circuit is at the first logical level and the data in said memory element is in state "1" before said second operation is carried out, keeps the data in said data storage circuit at the first logical level when the data has not reached state "2", prevents the logical level in said data storage circuit from changing when the data in said memory element is in state "0" before said second operation is carried out, and keeps the data in said data storage circuit at the second logical level when the data in said data storage circuit is at the second logical level, and furthermore

said control circuit, in a third verify operation of verifying whether the data in said memory element has reached state "3", charges the data in said data storage circuit to the second logical level when the data in said data storage circuit is at the first logical level and the data has reached state "3", keeps the data in said data storage circuit at the first logical level when the data has not reached state "3", keeps the data in said data storage circuit at the second memory logical level when the data in said data storage circuit is at the second logical level, and carries out said second operation, second and third verify operations until the data in said data storage circuit has reached the second logical level.

12. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, judges whether the data in said memory element is in either state "2" or below or state "3" when the data in said memory element is read, stores the result of the judgment in said data storage circuit, thereafter judges whether the data is in either state "0" or state "1" or above, and, if the data stored in said data storage circuit is in state "3", charges the potential on the bit line connected to the memory element in which the data has been stored to a low level and keeps the potential of the bit lines connected to the memory elements whose data is in either state "1" or state "2" at a high level.

13. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit, in said second operation, omits the verify operation of verifying whether said data has reached state "3" in the first half of the verify operation of verifying whether said data has reached state "2" and omits the verify operation of verifying whether said data has reached state "2" in the latter half of the verify operation of verifying whether said data has reached state "3".

14. The nonvolatile semiconductor memory device according to claim 10, wherein

said control circuit sets an initial write voltage in changing the data in said memory element from state "0" to state "3" and in changing the data from state "1" to state "2" higher than an initial write voltage in changing the data in said memory element from state "0" to state "3".

15. A nonvolatile semiconductor memory device comprising:

a memory element which is connected to a bit line and a word line and stores one of state "0", state "1", state "2", and state "3" of data that differ in threshold voltage;

a data storage circuit which is connected to said bit line and stores the data read from said memory element; and

a control circuit which controls not only the potential on said bit line and that on said word line but also the operation of said data storage circuit, wherein

said control circuit operates in such a manner that

in a first read operation, the control circuit sets data of a first logical level in said data storage circuit when the data in said memory element is in either state "0" or state "1", and sets data of a second logical level in said data storage circuit when the data in said memory element is in either state "2" or state "3", and

that in a second read operation, the control circuit sets data of the first logical level in said data storage circuit when the data in said memory element is in either state

"0" or state "3", and sets data of the second logical level in said data storage circuit when the data in said memory element is in either state "1" or state "2".

16. The nonvolatile semiconductor memory device according to claim 15, wherein

said control circuit judges whether the data in said memory element is in either state "1" or below or state "2" or above in said first read operation and judges not only whether the data in said memory element is in either state "0" or state "1" or above but also whether the data is in either state "2" or below or state "3" in said second read operation.

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